

DERWENT-ACC-NO: 1992-136975

DERWENT-WEEK: 199217

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TITLE: IC device with built-in EPROM has  
polyimide layer - as passivation laid on area excluding  
etched trench above gate electrode of memory transistor  
to ease thermal stress NoAbstract Dwg 1/2

PATENT-ASSIGNEE: NEC CORP[NIDE]

PRIORITY-DATA: 1990JP-0191743 (July 19, 1990)

PATENT-FAMILY:

PUB-NO	PAGES	PUB-DATE	
LANGUAGE		MAIN-IPC	
<b>JP 04078173 A</b>		March 12, 1992	N/A
002	N/A		

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
APPL-DATE		
JP 04078173A	N/A	
1990JP-0191743	July 19, 1990	

INT-CL (IPC): H01L021/31, H01L027/11 , H01L029/78

ABSTRACTED-PUB-NO:

EQUIVALENT-ABSTRACTS:

TITLE-TERMS: IC DEVICE BUILD EPROM POLYIMIDE LAYER  
PASSIVATION LAY AREA EXCLUDE  
ETCH TRENCH ABOVE GATE ELECTRODE MEMORY  
TRANSISTOR EASE THERMAL  
STRESS NOABSTRACT

ADDL-INDEXING-TERMS:

INTEGRATED CIRCUIT

DERWENT-CLASS: A85 L03 U11 U13 U14

CPI-CODES: A05-J01B; A12-E07C; L03-G04A; L04-C12E;

EPI-CODES: U11-C05A; U11-C05B9; U13-C04A; U14-A03B7;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C1992-063667

Non-CPI Secondary Accession Numbers: N1992-102210